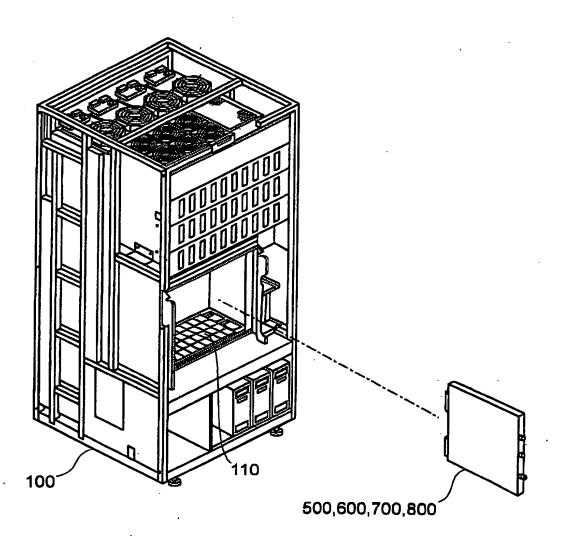
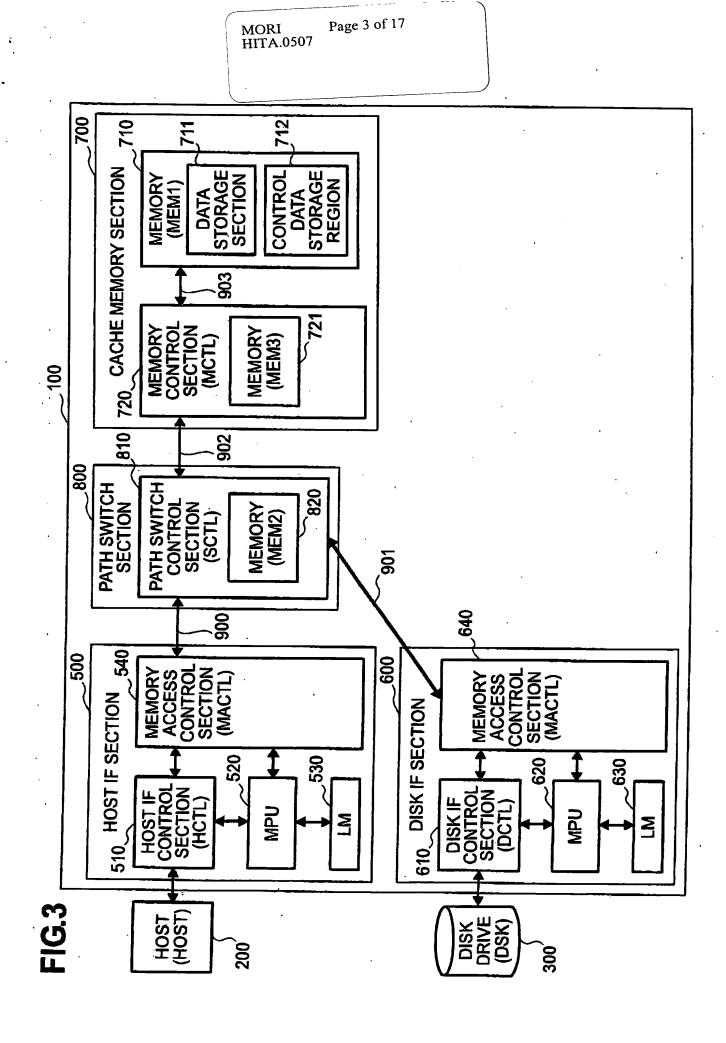


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FIG.2





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ACCESS/NO ACCESS TO MEMORY IN MEMORY CONTROL SECTION TARGET NODE(ENTIRE MPU COMMUNICATIONS, SPECIFIC MPU ID OF ADDRESSEE IF SECTION (e.g., 64 IF SECTIONS: 0-63(EACH IF SECTION), 128(EVERY IF SECTION), 255(MEMORY SECTION)) COMMUNICATIONS, CACHE MEMORY COMMUNICATIONS ACCESS/NO ACCESS TO MEMORY IN SWITCH DATA TYPE(CONTROL DATA OR DATA) ACCESSING ADDRESS e.g., MEMORY DATA SECTION(12) ID OF ADDRESSER IF SECTION **ACTUAL DATA/CONTROL DATA ACCESSING DATA LENGTH** PRIORITY INFORMATION DETAILS DATA/CONTROL DATA COMMUNICATIONS **ACCESS ADDRESS** LESS-BROAD CLASSIFICATION ADDRESSER ID ADDRESSEE ID **DATA LENGTH ATTRIBUTE** CLASSIFICATION HEADER SECTION(11) DATA SECTION SECTION HEADER BROAD

DATA PROTECTION CODE

CHECK CODE

FIG5

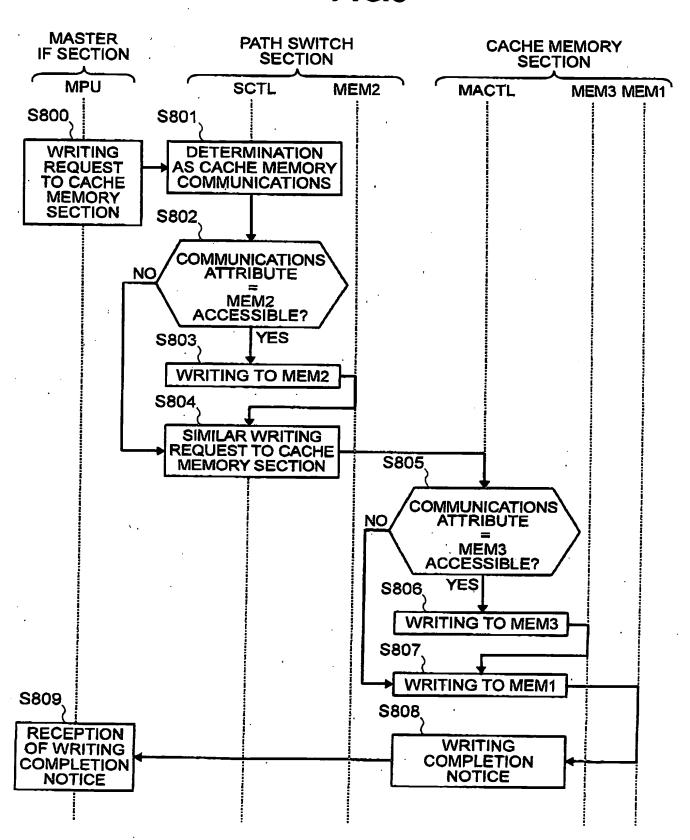
**FIG.6** 

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FIG.7 **MASTER** PATH SWITCH **CACHE MEMORY** IF SECTION SECTION SECTION MPU SCTL MEM2 **MACTL** MEM3 MEM1 **S700** S701 READING DETERMINATION REQUEST OF AS CACHE MEMORY CONTROL DATA COMMUNICATIONS TO CACHE MEMORY SECTION COMMUNICATIONS ATTRIBUTE NO MEM2 ACCESSIBLE? YES S702 **S703 HIT ACKNOWLEDGE** TO MEM2 **S704** NO HIT? YES **S705** TRANSMISSION OF HIT CONTROL DATA **S707 READING REQUEST S708** OF CONTROL DATA COMMUNICATIONS NO **ATTRIBUTE** MEM3 ACCESSIBLE? YES S709 HIT ACKNOWLEDGE TO MEM3 S710 NO HIT? YES S711 TRANSMISSION OF HIT CONTROL DATA **S712 READING OF** CONTROL **DATA FROM MEM1 S713 S706** TRANSMISSION **RECEPTION OF** CONTROL DATA OF CONTROL DATA **READ FROM MEM1** 

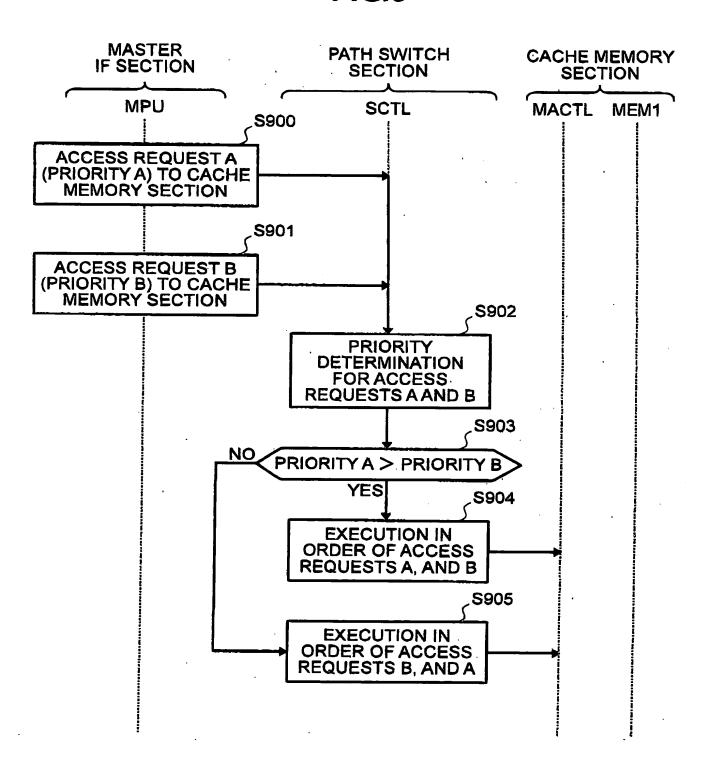
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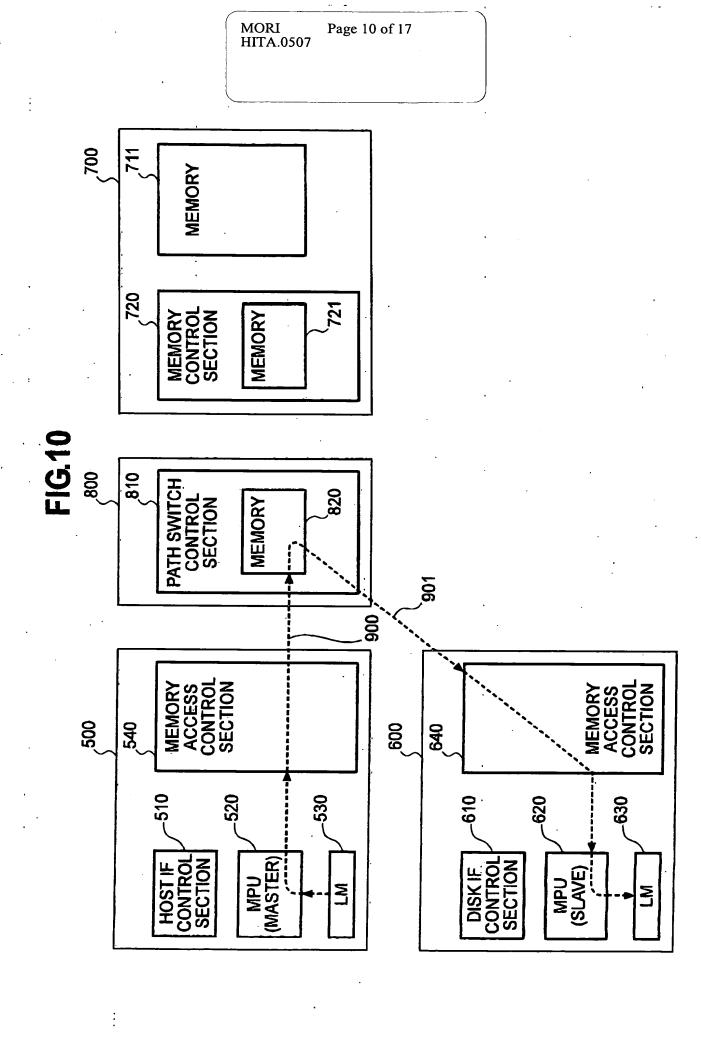
FIG.8



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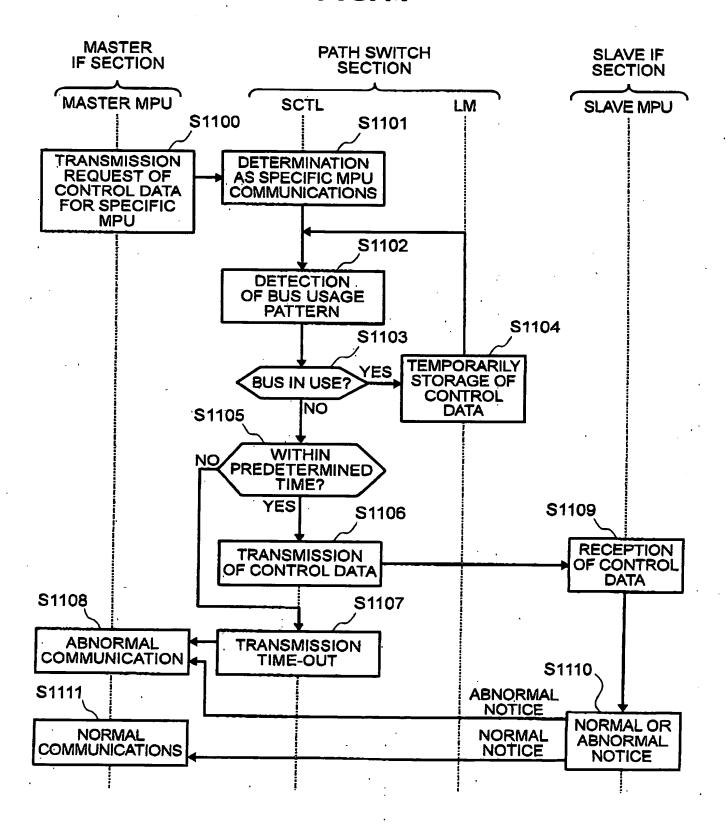
FIG.9

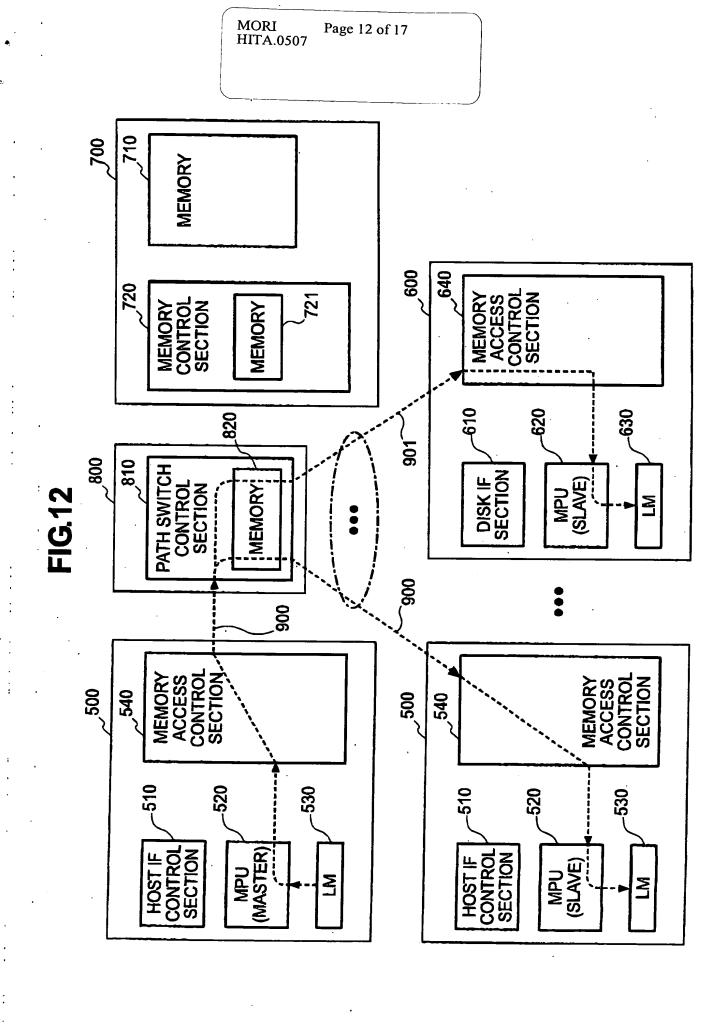




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**FIG.11** 





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**FIG.13** 

